UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/692,073	10/19/2000	Coke Reed	F.11146	6301

7590 01/18/2006

KEITH D. NOWAK
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
1177 AVENUE OF THE AMERICAS
41ST FLOOR
NEWYORK, NY 10036-2714

EXAMINER	
PHAN, TRI H	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/692,073	REED ET AL.	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/4/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,13,16,17,19 and 20* is/are rejected.

7)☒ Claim(s) *4,11,12,14,15 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/4/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Arguments

1. This Office Action is in response to the Response/Amendment filed on October 4th, 2005. Claim 10 is now canceled and new claims 19-20 are added. Claims 1-9 and 11-20 are now pending in the application.

Information Disclosure Statement

2. The information disclosure statement filed October 4, 2005, fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of the non-patent literature publication (Roche et al., "Performance of Congestion Control Mechanisms In Wormhole Routing Networks", Proceedings of the IEEE Infocom 1997, The Conference on Computer communications. 16th Annual Joint Conference of the IEEE Computer and Communications societies. Driving the Information Revolution. Kobe, Los Alamitos, California, U.S.A., Vol. 3; April 1997) or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Objections

3. Claims 7-9, 13-14, and 16-18 are objected to because of the following informalities:

Regarding claim 7, line 6, the word "*form*" after the phrase "sending data" is a typographical error; it should be correct to -- from --.

Regarding claim 8, line 5, the word "*the*" in front of the term "level of" should be correct to -- a -- for clarity.

Regarding claim 9, line 2, the word "*the*" in front of the phrase "distinct first, second,..." should be deleted for clarity.

Regarding claim 9, the word "*fifth*" after the phrase "all input ports of the" (line 17) is a typographical error; it should be correct to -- first --; and the term "a message" (line 17) should be correct to – the messages --.

Regarding claim 13, line 2, the word "*the*" in front of the phrase "first, second,.." should be deleted for clarity.

In regard to claim 13, the word "*a*" in front of the term "first message" (lines 12 and 13) should be correct to -- the -- for clarity.

Regarding claim 13, the word "*a*" in front of the term "second message" (line 14) should be correct to -- the -- for clarity.

In regard to claim 14, the word "*a*" in front of the term "second message" (line 2) and the word "*a*" in front of the term "first message" (line 3) should be correct to -- the -- for clarity.

Also in claim 14, line 4, the word "*seventh*" in front of the word "node" should be correct to -- fourth --.

Regarding claim 16, the word "*the*" after the term "simultaneously" (line 9) should be correct to -- a -- for clarity.

Regarding claim 17, the word "*a*" in front of the term "second input port" (line 10) should be correct to -- the -- for clarity.

In regard to claim 18, the word "*a*" in front of the term "second message" (line 2) and the word "*a*" in front of the term "first message" (line 3) should be correct to -- the -- for clarity.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-4 and 19-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1, lines 12-14 state "*no node exists in the interconnect structure that can have data routed directly to it from both the first node and the second node*". This is not supported in the specification or the drawings. For example, in figures 3A-C, 6A-C and 7-8; data can be routed directly to node C from both node A and node B (see figures 6A-C, 7); or data can be routed to node A or node H directly from node B and C. This contradicts the limitation in claim 1 as node A or node H clearly can have data routed directly to it from node B (or node C) as the first node and node C (or node B) as the second node.

Claim 2, lines 8-10 state "*no node exists in the interconnect structure that can receive data directly routed both from the first node and the third node*". This is also not supported in the specification or the drawings. Figure 8 again shows data being routed directly to node B or node

C from a plurality of nodes such as node D, E, U, V, W, and node X (as first, second and third nodes).

It also notes that claim 19 is further disclosed "*a plurality of messages simultaneously enter a third node*", e.g. "*third node*" simultaneously receives a plurality of messages.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 17-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 17, the last limitation of claim 17 states, "... *there is a path through the second output port to a target destination for the second message and a path through the first output port to a target destination for the second message.*" Are both first and second outputs supposed to output the second message and if so, what happens to the first message?

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, 5-9, 13, 16-17, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Reed, Coke S.** (U.S.6,272,141; hereinafter refer as '**Coke**') in view of **Hesse, John E.** (U.S.6,289,021; hereinafter refer as '**Hesse**').

Note: The recited limitation "... *and no node exists in the interconnect structure*..." in claims 1-2, is a negative limitation; therefore, the limitations following the term are not considered in the claimed limitation. It is suggested applicant amends the term into positive limitation and to overcome the rejection under 35 U.S.C. 112, first paragraph, as disclosed in part 5 above in this office action.

- In regard to claim 1, Reed discloses, *an interconnect structure, comprising a plurality of interconnected nodes, including a first node and a second node* (nodes 102 in the multiple different levels interconnect structure in figures 1A-D, e.g. "*first and second nodes*"); *the first node having a plurality of data input ports, a plurality of data output ports, and a control signal input port and the second node having a plurality of data input ports, a plurality of data output ports, and a control signal output port* (figure 2; col. 8, lines 46-52; wherein each node 102 has a plurality of inputs/outputs ports and control input/output ports, e.g. data inputs/outputs and control input/output) *and a routing logic associated with the nodes*(col. 20, lines 24-28 where this is describing a generic node setup), *the routing logic for routing data selectively among the interconnected nodes* (col. 8, lines 52-55); *the first and second nodes being positioned in the interconnect structure so that the first node cannot route data to the second node, the second node cannot route data to the first node* (figure 3A, where it is clear from the data path lines that

element 324 cannot route data to element 322 or 332; where element 332 or "*first node*" cannot route data to element 320 or "*second node*", and vice versa); *and a logic included as part of said routing logic and associated with the first node that uses information concerning routing of data through the second node to route data through the first node* (col. 8, lines 52-55 whereby communicating control of transmission message data with other nodes by a given node allows elements 320 and 332 to communicate this control information with each other as well)".

However, Reed lacks what Hesse discloses about a scalable low-latency switch for usage in a multiple level interconnection structure (for example see figures 1A-C); *wherein at least one of the plurality of nodes is adapted to simultaneously receive a plurality of messages* (for example see col. 6, lines 59-64; col. 5, lines 10-17; where messages are simultaneously inserted into different columns of the chip in the scalable low-latency switch).

It would have been obvious to one with ordinary skill in the ad at the time of invention to implement multiple columns' chip into the switch for the purpose of simultaneously receiving messages at the switch or node. The motivation for implementing multiple column's chip into the switch is so that each switch can receives concurrent message paths at a time and thus preventing data contention (Hesse, col. 1, lines 29-32).

- Regarding claim 2, in addition to features in base claim 1 (see rationales pertaining the rejection of base claim 1 discussed above), Reed further discloses *wherein the plurality of interconnected nodes includes a third node distinct from the first and second nodes* (nodes 102 in the multiple level interconnect structure in figures 1A-D; wherein nodes are distinct from different levels), *the third node having a plurality of data input ports, a plurality of data output*

ports, and a control signal output port (for example see figures 2, 3A-B; wherein each node 102 has a plurality of inputs/outputs ports and control input/output ports, e.g. data inputs/outputs and control input/output as disclosed in figure 2 and where the dashed line with arrow, e.g. "*control signal output*", connecting element 330 to 320 and 332 indicates the direction of the control message flow in figure 3A-B); *and the first and third nodes are positioned in the interconnect structure so that the first node cannot route data to the third node, the third node cannot route data through the first node* (for example see figures 3A-C where element 332 acts as applicant's "*first node*" and cannot route data to element 330 acts as applicant's "*third node*"); *and the logic associated with the first node uses information concerning routing of data through the third node to route data through the first node* (col. 8, lines 52-55 whereby communicating control of transmission message data with other nodes by a given node allows elements 320, 330 and 332 to communicate this control information with each other as well).

- In regard to claim 3, in addition to features in base claims 1 and 2 (see rationales pertaining the rejection of base claims 1 and 2 discussed above), Reed fails to explicitly disclose about another different level in the figures 3A-C, such as Level J-2. However, it is obvious that, in the multiple level interconnect structure as disclosed in figures 1A-D and 4; the level such as Level J-2 is just another level, e.g. level J=3 in figure 4 of the multiple level interconnect structure; *wherein the plurality of interconnected nodes includes a fourth node distinct from the first, second, and third nodes* (nodes 102 in the multiple level interconnect structure in figures 1A-D; wherein nodes are distinct from different levels), *the fourth node having a plurality of data input ports, a plurality of data output ports, and a control signal output port*

(figure 2; col. 8, lines 46-52; wherein each node 102 has a plurality of inputs/outputs ports and control input/output ports, e.g. data inputs/outputs and control input/output); *and a logic associated with fourth node included as part of the routing logic* (col. 20, lines 24-28 where this is describing a generic node setup) *being capable of sending a first control signal to the first node* (col. 8, lines 52-55; wherein the dashed line such as the ones in figure 3A-C indicates the direction of the control message flow), *the first control signal containing information concerning routing possibilities through the fourth, third and second nodes, and the logic associated with the first node for routing of data through the first node depending at least in part on information concerning routing of data through the fourth, third and second nodes* (col. 8, lines 52-55 whereby communicating control of transmission message data with other nodes by a given node allows elements in different levels to communicate this control information with each other as well).

- Regarding claim 5, Reed discloses, *an interconnect structure, comprising a plurality of nodes including distinct first, second, and third nodes and a plurality of interconnect lines selectively coupling the nodes of the interconnect structure* (nodes 102 with the interconnect lines 104 in the multiple different levels interconnect structure in figures 1A-D, e.g. "*first, second and third nodes*"), *the first and second nodes being both positioned to send data to the third node* (figure 3A, element 332 acts as applicant's first node, element 320 acts as applicant's second node, and element 326 acts as applicant's third node); *a control signal carrying line connected from the second node to the first node for carrying control signals from the second node to the first node* (figures 3A-C where the dashed line with arrow, e.g. "*control signal*

carrying line", connecting element 320 to 332 indicates the direction of the control message flow); *and a routing logic associated with the second node capable of sending data to the third node and sending a control signal to the first node that can inform the first node that the first node is allowed to send a message to the third node* (col. 8, lines 52-55 whereby communicating control of transmission message data with other nodes by a given node allows elements 320 and 332 to communicate this control information with each other as well).

However, Reed lacks what Hesse discloses about a scalable low-latency switch for usage in a multiple level interconnection structure (for example see figures 1A-C); *wherein at least one of the plurality of nodes is adapted to simultaneously receive a plurality of messages* (for example see col. 6, lines 59-64; col. 5, lines 10-17; where messages are simultaneously inserted into different columns of the chip in the scalable low-latency switch).

It would have been obvious to one with ordinary skill in the ad at the time of invention to implement multiple columns' chip into the switch for the purpose of simultaneously receiving messages at the switch or node. The motivation for implementing multiple columns' chip into the switch is so that each switch can receives concurrent message paths at a time and thus preventing data contention (Hesse, col. 1, lines 29-32).

- In regard to claim 6, in addition to features in base claim 5 (see rationales pertaining the rejection of base claim 5 discussed above), Reed further discloses wherein the third node has a plurality of input ports (for example see figure 2; col. 8, lines 46-52); but fails to explicitly disclose *wherein data from the first and second nodes arrive at the third node concurrently so that all of the input ports of the third node receive messages simultaneously*. Reed lacks what

Hesse discloses about a scalable low-latency switch for usage in a multiple level interconnection structure (for example see figures 1A-C); *wherein data ... arrive ... concurrently so that all of the input ports of the third node receive messages simultaneously* (for example see col. 6, lines 59-64; col. 5, lines 10-17; where messages are simultaneously inserted into different columns of the chip, e.g. "*third node*", in the scalable low-latency switch).

It would have been obvious to one with ordinary skill in the ad at the time of invention to implement multiple columns' chip into the switch for the purpose of simultaneously receiving messages at the switch or node. The motivation for implementing multiple columns' chip into the switch is so that each switch can receives concurrent message paths at a time and thus preventing data contention (Hesse, col. 1, lines 29-32).

- Regarding claims 7-8, in addition to features in base claims 5-6 (see rationales pertaining the rejection of base claims 5-6 discussed above), Reed further discloses about the *plurality of nodes includes distinct first, second, third, fourth, fifth, sixth, and seventh nodes in the hierarchical interconnect structure* (nodes 102 with the interconnect lines 104 in the multiple different levels interconnect structure in figures 1A-D and 4, e.g. "*first, second, third, fourth, fifth, sixth, and seventh*"; wherein the figures 3A-C with the outside, level J, level J-1, and so on, disclose the hierarchical level in the interconnect structure); but fails to explicitly disclose *wherein the third node is capable of simultaneously sending data from the first node to the fourth node, and capable of sending data from the second node to the seventh node.* Reed lacks what Hesse discloses about a scalable low-latency switch for usage in a multiple level interconnection structure (for example see figures 1A-C); *wherein the third node is capable of simultaneously*

sending data ... and capable of sending data ... (for example see col. 6, lines 59-64; col. 5, lines 10-17; where messages are simultaneously inserted into different columns of the chip in the scalable low-latency switch, thus providing many concurrent message paths from any input to any output).

It would have been obvious to one with ordinary skill in the ad at the time of invention to implement multiple columns' chip into the switch for the purpose of simultaneously receiving messages at the switch or node. The motivation for implementing multiple columns' chip into the switch is so that each switch can provide concurrent message paths from any input to any output at a time and thus preventing data contention (Hesse, col. 1, lines 29-32).

- In regard to claim 9, Reed discloses, *an interconnect structure, comprising a plurality of nodes adapted to generate control signals including the distinct first, second, and third nodes, and a collection of interconnect lines selectively coupling the nodes* (nodes 102 with the interconnect lines 104 in the multiple different levels interconnect structure in figures 1A-D, e.g. "*first, second and third nodes*"); *the third node having a plurality of message input ports* (figure 2; col. 8, lines 46-52; wherein each node 102 has a plurality of inputs/outputs ports), *the first and second nodes positioned in the structure so that the first node can route a data packet to the third node; the second and third nodes positioned in the structure so that the second node can route a data packet to the third node* (figure 3A, element 332 acts as applicant's first node, element 320 acts as applicant's second node, and element 326 acts as applicant's third node); *the first and second nodes positioned in the network so that the second node can send a control signal to the first node* (figures 3A-C where the dashed line with arrow, e.g. "*control signal*", connecting

element 320 to 332 indicates the direction of the control message flow); *a routing logic at the first node* (col. 20, lines 24-28 where this is describing a generic node setup) *using the control signal from the second node to route messages* (col. 8, lines 52-55); *the second node routing a first message to the third node and the first node A routing a second message to the third node* (for example see figures 3A-C).

However, Reed lacks what Hesse discloses *wherein the second message concurrently arrives with the first message and all input ports of the third node concurrently receiving the messages* (for example see col. 6, lines 59-64; col. 5, lines 10-17; where messages are simultaneously inserted into different columns of the chip, e.g. "*third node*", in the scalable low-latency switch).

It would have been obvious to one with ordinary skill in the ad at the time of invention to implement multiple columns' chip into the switch for the purpose of simultaneously receiving messages at the switch or node. The motivation for implementing multiple columns' chip into the switch is so that each switch can provide concurrent message paths from any input to any output at a time and thus preventing data contention (Hesse, col. 1, lines 29-32).

- Regarding claims 13 and 16, Reed discloses, *an interconnect structure, comprising a plurality of interconnected nodes including the first, second, third, fourth, and fifth nodes* (nodes 102 with the interconnect lines 104 in the multiple different levels interconnect structure in figures 1A-D, e.g. "first, second, third, fourth, and fifth nodes"), *each of the first, second, third, fourth, and fifth nodes having a plurality of input ports and a plurality of output ports* (figure 2; col. 8, lines 46-52; wherein each node 102 has a plurality of inputs/outputs ports), *and third node*

being positioned to receive messages from the first and second nodes and to route messages to the fourth and fifth nodes (figure 3A, element 324 acts as applicant's first node, element 322 acts as applicant's second node, element 320 acts as applicant's third node, element 326 acts as applicant's fourth node and element 328 acts as applicant's fifth node; wherein the third node receives message from the first and second nodes and to route message to the fourth and fifth nodes); *a plurality of interconnect structure output ports including an output port that is accessible from the third node but not the fifth node* (figure 3A where the third node routes the message to the fourth node through the interconnect line connecting between the third node and the fourth node, but not the interconnect line connecting between the third node and the fifth node).

Reed does disclose about *the routing logic included within the interconnect structure* (col. 20, lines 24-28 where this is describing a generic node setup) *where the third node can route a first message through the fourth node to a target interconnect structure output port for a first message and can route the second message through the fifth node to a target interconnect structure output port for the second message* (figure 3A where the element 320 routes the message from the element 322 to the element 326 through the interconnect line connecting between the element 320 and 326, e.g. "*target interconnect structure output port for a first message*", and routes the message from the element 324 to the element 328 through the interconnect line connecting between the element 320 and the element 328, e.g. "*target interconnect structure output port for the second message*"; which also discloses in figure 7; col. 10, line 56 through col. 11, line 3), but lacks what Hesse discloses *where the first and second nodes concurrently send a first and second messages to the third node, and wherein at least one*

of the plurality of nodes is adapted to simultaneously receive a plurality of messages (for example see col. 6, lines 59-64; col. 5, lines 10-17; where messages are simultaneously inserted into different columns of the chip, e.g. "*third node*", in the scalable low-latency switch; thus, provide concurrent message paths from any input to any output at a time).

It would have been obvious to one with ordinary skill in the ad at the time of invention to implement multiple columns' chip into the switch for the purpose of simultaneously receiving messages at the switch or node. The motivation for implementing multiple columns' chip into the switch is so that each switch can provide concurrent message paths from any input to any output at a time and thus preventing data contention (Hesse, col. 1, lines 29-32).

- In regard to claim 17, Reed discloses, *an interconnect structure* (see the multiple level interconnect structure in figures 1A-D) *for carrying message packets consisting of a header and a payload with header indicating a target output port* (for example see figure 18) *comprising a plurality of interconnected nodes* (nodes 102 in the multiple different levels interconnect structure in figures 1A-D) *including a first node having first and second input ports and first and second output ports* (for example see figure 2); *a plurality of output ports that are accessible from the first input port but not from the first output port* (figure 3A where the element 320 routes the message from the element 322 to the element 326 through the interconnect line connecting between the element 320 and 326, e.g. "*first output port*", but not routes the message from the element 324 to the element 328 through the interconnect line connecting between the element 320 and the element 328, e.g. "*first input port*"; which also discloses in figure 7; col. 10, line 56 through col. 11, line 3). Reed does disclose about *the routing logic included within the*

interconnect structure (col. 20, lines 24-28 where this is describing a generic node setup), *and there is a path through the second output port to a target destination for the second message and a path through the first output port to a target destination for the second message* (figure 3A where the element 320 routes the message from the element 322 to the element 326 through the interconnect line connecting between the element 320 and 326, e.g. "*target destination for a first message*", and routes the message from the element 324 to the element 328 through the interconnect line connecting between the element 320 and the element 328, e.g. "*target destination for the second message*"; which also discloses in figure 7; col. 10, line 56 through col. 11, line 3), but lacks what Hesse discloses *where the first and second messages simultaneously arrives at the first and the second input ports* (for example see col. 6, lines 59-64; col. 5, lines 10-17; where messages are simultaneously inserted into different columns of the chip in the scalable low-latency switch, thus providing many concurrent message paths from any input to any output).

It would have been obvious to one with ordinary skill in the ad at the time of invention to implement multiple columns' chip into the switch for the purpose of simultaneously receiving messages at the switch or node. The motivation for implementing multiple columns' chip into the switch is so that each switch can provide concurrent message paths from any input to any output at a time and thus preventing data contention (Hesse, col. 1, lines 29-32).

- Regarding claims 19-20, in addition to features in base claim 1 (see rationales pertaining the rejection of base claim 1 discussed above), Reed further discloses *wherein one of the plurality of messages entering the third node is sent to a fourth node on the same level as the*

third node and another of the multiple messages entering the third node is sent to a fifth node on a level below the third node (figure 3A where the element 320, e.g. "*third node*", routes the message from element 322 to the element 326, e.g. "*fourth node*", through the interconnect line connecting between the element 320 and 326, e.g. "*on the same level as the third node*", and routes the message from the element 324 to the element 328, e.g. "*fifth node*", through the interconnect line connecting between the element 320 and the element 328, e.g. "*on a level below the third node*"; which also discloses in figure 7; col. 10, line 56 through col. 11, line 3), but lacks what Hesse discloses *where a plurality of messages simultaneously enter a third node* (for example see col. 6, lines 59-64; col. 5, lines 10-17; where messages are simultaneously inserted into different columns of the chip, e.g. "*third node*", in the scalable low-latency switch; thus, provide concurrent message paths from any input to any output at a time).

It would have been obvious to one with ordinary skill in the ad at the time of invention to implement multiple columns' chip into the switch for the purpose of simultaneously receiving messages at the switch or node. The motivation for implementing multiple columns' chip into the switch is so that each switch can provide concurrent message paths from any input to any output at a time and thus preventing data contention (Hesse, col. 1, lines 29-32).

Response to Amendment/Arguments

10. Applicant's arguments filed on July 7th, 2005 with respect to claims 1-3, 5-7 and 9 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

11. Claims 4, 11-12, 14-15, and 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten or amended to overcome the objection(s), the rejection(s) under 35 U.S.C. 112, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hesse, John (U.S.6,754,207), **Carvey, Philip P.** (U.S6,947,433) and **Dally et al.** (U.S.6,285,679) are all cited to show devices and methods for improving switching technique in the telecommunication architectures, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (571) 272-3074. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on (571) 272-3126.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(571) 273-8300

Hand-delivered responses should be brought to Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRIAN NGUYEN
PRIMARY EXAMINER

Tri H. Phan
January 13, 2006